IN THE CLAIMS

1.(Previously Presented) A semiconductor die comprising:

a conductive test signal bump for transmitting test signals off of said semiconductor die;

a test signal redistribution layer trace for communicating said test signals to said conductive test signal bump, wherein said test signal redistribution trace is included in a redistribution layer and said test signal redistribution trace is disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within said die and along said test signal redistribution layer trace, said test signal redistribution layer trace communicatively coupled to said conductive test signal bump; and

a test probe point for accessing said test signals in said semiconductor die and for electrical coupling to said redistribution layer.

2.(Original) The semiconductor die of Claim 1 wherein said semiconductor die is a flip chip die configured for connection to a package substrate such that said conductive test signal bump is electrically coupled to an external access point of said package substrate.

3.(Original) The semiconductor die of Claim 1 wherein said test probe point is

accessible by drilling from a first surface of said semiconductor die.

4.(Currently Amended) The semiconductor die of Claim 1 wherein said test probe point comprises a focused ion beam (FIB) pad accessible by focused ion beam drilling and conductive material backfill, wherein said FIB pad is communicatively coupled to said test signal redistribution layer trace by said conductive material backfill.

5.(Currently Amended) The semiconductor die of Claim 1 wherein said test signal redistribution layer trace is dedicated for test signals ~~Claim 4 wherein said FIB pad is communicatively coupled to said test signal redistribution layer trace by said conductive material backfill~~.

6.(Previously Presented) The semiconductor die of Claim 1 wherein said test signal redistribution layer trace is routed in a spiral pattern.

7.(Original) The semiconductor die of Claim 1 wherein said test signal redistribution layer trace is routed in a spiral pattern with conductive fingers located in positions such that drilling and conductive material backfill provides access to internal signals for testing at various electronic component

configuration granularity.

8.(Withdrawn) A semiconductor fabrication method:

forming electronic components on said semiconductor die;

forming a test probe point in said semiconductor die for access by drilling and conductive material backfill;

depositing a test signal redistribution layer trace comprising conductive traces on said semiconductor die in a redistribution layer; and

fabricating a conductive test signal bump for conveying a test signal to an external access point on a package substrate, said conductive test signal bump located on a first surface of said semiconductor die and electrically coupled to said signal redistribution layer.

9. (Withdrawn) The method of Claim 8 wherein said semiconductor die is a flip chip die configured for connection to said package substrate such that said conductive test signal bump is electrically coupled to a test signal access component of said package substrate, said test signal access component coupled to said external access point.

10. (Withdrawn) The method of Claim 8 wherein said conductive traces are

disposed such that multiple test signals are accessible for testing at various electronic component configuration granularity.

11. (Withdrawn) The method as recited in Claim 8 further comprising accessing said test signal at said external access point.

12. (Withdrawn) The method as recited in Claim 8 wherein said test signal redistribution layer trace comprises a spiral pattern a plurality of conductive fingers extending from said conductive traces, such that various electronic component configuration granularity over large areas of said semiconductor die is accessible for testing.

13.(Previously Presented) A semiconductor device comprising:

a package substrate for communicating test signals on an external access point, wherein said package substrate includes a conductive trace disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within said package substrate and along said conductive trace; and

a semiconductor die having test probe points accessible by said external access point, wherein said semiconductor die is electrically coupled to said

package substrate.

14.(Original) The semiconductor device of Claim 13 wherein said package substrate comprises:

a first surface with ball grid array;

a second surface with conductive contacts for electrically coupling with conductive bumps of said semiconductor die, including a conductive contact for electrically coupling with a conductive test signal bump; and

a trace for electrically coupling one of said conductive contacts to said external access point.

15.(Previously Presented) The semiconductor device of Claim 13 wherein said semiconductor die comprises:

a conductive test signal bump for transmitting internal test signals off of said semiconductor die to said package substrate, said conductive test signal bump located on a first surface of said semiconductor die and electrically coupled to said signal redistribution layer;

a redistribution layer including a test signal redistribution layer trace for communicating internal signals to said conductive test signal bump, said signal redistribution layer communicatively coupled said conductive test signal bump;

a test probe point for accessing test signals in said semiconductor die and for electrical coupling to said signal redistribution layer; and

a test access via for electrically coupling said test probe point to said signal redistribution layer.

16.(Original) The semiconductor device of Claim 15 wherein said test probe point comprises a focused ion beam (FIB) pad accessible by focused ion beam drilling and conductive material backfill.

17.(Original) The semiconductor device of Claim 15 wherein said test signal redistribution layer trace is routed in patterns in which trace widths and spacing between redistribution layer traces are minimized without causing signal interference.

18.(Original) The semiconductor device of Claim 14 wherein said external access point is accessible by automatic test equipment.

19. (Withdrawn) A semiconductor test process comprising:

determining a boring location aligned to a test signal redistribution layer trace and a test probe point in a semiconductor die;

boring a hole to said test probe point in a first surface of said semiconductor die;

backfilling said hole with conductive material to couple said signal redistribution layer and said test probe point;

coupling electrically a test signal conductive bump on said first surface of said semiconductor die to a conductive component of a second surface of said package substrate, wherein said conductive bump is electrically coupled to said test signal redistribution layer trace; and

measuring test signals at an external access point of said package substrate.

20. (Withdrawn) The process of claim 18 wherein said test probe point is electrically coupled to a particular signal trace in said semiconductor die.

21. (Withdrawn) The process of claim 18 wherein said test signal is an internal semiconductor die signal while said semiconductor die is operating.

22. (Withdrawn) The process of claim 18 wherein said measuring is performed by automatic test equipment.

23. (Withdrawn) The process of claim 18 wherein test signal redistribution layer trace is routed in a spiral pattern.

24. (Withdrawn) The process of claim 23 wherein said signal redistribution layer further comprises a plurality of conductive fingers extending from said plurality of conductive traces, such that a larger area of said semiconductor die is accessed.

25. (Withdrawn) The process of claim 18 wherein said boring and said backfilling are performed using a focused ion beam (RB).

26. (Withdrawn) An electronic system comprising:

a processing flip chip device for processing information, wherein said flip chip device includes a test probe point for accessing a semiconductor die internal signal of said processing flip chip through a test signal redistribution layer trace and an external access point on a package substrate;

a bus for communicating information to said processing flip chip device, said bus coupled to said processing flip chip device; and

a memory for storing said information, said memory coupled to said bus.

27. (Withdrawn) The electronic system of Claim 26 wherein said package substrate comprises:

a first surface with a ball grid array;

a second surface with conductive contacts for electrically coupling with conductive bumps of said semiconductor die, including a conductive test signal bump; and

a trace for electrically coupling one of said conductive contacts to said external access point.

28. (Withdrawn) The electronic system of Claim 26 wherein said semiconductor die

comprises:

a conductive test signal bump for transmitting internal test signals off of said semiconductor die;

a test signal redistribution layer trace for communicating said internal test 15 signals to said conductive test signal bump, wherein said test signal redistribution trace is included in a redistribution layer, said test signal redistribution layer trace communicatively coupled to said conductive test signal bump;

a test probe point for accessing internal test signals in said semiconductor

20 die and for electrical coupling to said redistribution layer.

29. (Withdrawn) The electronic system of Claim 28 wherein said probe point comprises a focused ion beam (FIB) pad accessible by focused ion beam drilling and conductive material backfill.

30. (Withdrawn) The electronic system of Claim 26 wherein said processing flip chip device is for processing game console information.

31. (Withdrawn) The electronic system of Claim 26 wherein said processing flip chip device is for processing graphics information.

32. (Withdrawn) The electronic system of Claim 26 wherein said processing flip chip device is for processing communication information.

33. (Withdrawn) The electronic system of Claim 32 wherein said processing flip chip device is for processing cell phone information.

34. (Withdrawn) The electronic system of Claim 26 wherein said processing flip chip device is for processing information in a computer system.

35. (Withdrawn) The electronic system of Claim 26 wherein said processing flip chip device is for processing personal digital assistant information.